

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

*I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to Commissioner of Patents and Trademarks, Washington, D.C. 20231 on*

March 15, 2000  
date

Linda S. Botter  
Signature



Applicant : Broadcom Corporation  
For : Reissue of U.S. Patent No. 5,604,741  
Issued : February 18, 1997  
Title : ETHERNET SYSTEM  
Application No. : 09/252,551  
Filed : February 18, 1999  
  
Docket No. : 34176/JWE/B600

REISSUE DECLARATION AND POWER OF ATTORNEY

BOX REISSUE  
Assistant Commissioner for Patents  
Washington, D.C. 20231

P.O. Box 7068  
Pasadena, Ca. 91109-7068  
March 10, 2000

Commissioner:

We, Henry Samueli, Mark Berman and Fang Lu, the below named inventors, hereby declare and state as follows:

1. Our respective Post Office address and citizenship are as stated below next to our respective names.
2. We believe that we are the original, first and joint inventors of the subject matter which is described and claimed in original Letters Patent No. 5,604,741 (the '741 patent") and in the reissue specification and claims, comprising Reissue Application Serial No. 09/252,551, filed February 18, 1999, for which invention we request a reissue patent.

**Application No. Reissue of U.S. Patent No. 5,604,741**

3. We have reviewed and understand the contents of the above-identified specification including the claims as amended by the amendment referred to below.
4. We acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).
5. We believe that the original U.S. Patent No. 5,604,741 which issued on our Application No. 08/398,759 is partly "inoperative" by reason of having claimed less than we had a right to claim in the original Letters Patent.
6. The error arose in failure to present claims having the scope and language of original new claims 104-144 presented in the attached reissue application, in that the communication system processes communication signals in a novel fashion disclosed in the specification, and is usable in a general multi-pair communication environment not necessarily including a computer and a hub.
7. The error was discovered in late 1998 as plans evolved for the production of new designs. At that time, U.S. Patent No. 5,604,741 was reviewed in conjunction with the new designs and it was realized that one important embodiment of the invention was the use of digital equalization in a multi-pair communication environment, as set forth in the specification, and that the patent claimed less than we had a right to claim. In addition, error arose in that we did not appreciate the nature and scope of claims which could have been presented in our original application, and since we are inexperienced with United States patent laws, we did not appreciate that the claims may not have included subject matter to which we were entitled. It is now our belief that we are entitled to a scope of protection defined by original claims 104-144, which were not presented in the original application.

**Application No. Reissue of U.S. Patent No. 5,604,741**

8. We are informed and believe that the present newly added claims are to the same invention and of a scope which could have been made in our application which matured into the '741 patent. We are informed and believe that the conclusions reached about the errors with respect to original claims 104-144, not having been presented in the application, occurred as aforesaid after our patent issued, and are correct.
9. More specifically, the claims in the issued '741 patent are insufficient in failing to claim all that we that are entitled to claim for the following reasons:
- a. Claims 1-103 of the '741 are all apparatus claims calling for a system including at least a hub and a computer. The patent specification describes the invention as a system for and method of digitally processing communication signals in a multi-pair communication environment. In the summary of the invention (column 2, lines 2-45) the invention is described as comprising a digital adaptive equalizer of an advanced design which includes feedback techniques adapted to enhance the resolution provided by the equalizer in determining the amplitude levels of digital signals in a communications packet. The invention also includes circuits and techniques for extracting timing information from a received communication signal. The circuits and techniques do not depend upon the presence of either a hub or a computer for their novelty.
  - b. Newly added claims 104-129 are method claims directed to the techniques used to process communication signals and newly added claims 130-144 are directed to a bidirectional communication system not limited to one including a computer and hub.

**Application No. Reissue of U.S. Patent No. 5,604,741**

10. The errors specified herein, and all other errors being corrected in reissue application Serial No. 09/252,551 up to the filing of this declaration, occurred without any deceptive intent on the part of the undersigned applicants.

11. The reissue claims as presented herein are our invention as described in the original Letters Patent.

Applicants further appoint:

R. W. Johnston	(17,968)	John W. Eldredge	(37,613)	Gary J. Nelson	(44,257)
D. Bruce Prout	(20,958)	Gregory S. Lampert	(35,581)	Raymond R. Tabandeh	(43,945)
Hayden A. Carney	(22,653)	Grant T. Langton	(39,739)	Phuong-Quan Hoang	(41,839)
Richard J. Ward, Jr.	(24,187)	Constantine Marantidis	(39,759)	Kathy Mojibi	(41,409)
Russell R. Palmer, Jr.	(22,994)	Marilyn R. Khorsandi	(P-45,744)	Cynthia A. Bonner	(44,548)
LeRoy T. Rahn	(20,356)	Daniel R. Kimbell	(34,849)	Jun-Young E. Jeon	(43,693)
Richard D. Seibel	(22,134)	Craig A. Gelfound	(41,032)	Marc A. Karish	(44,816)
Walter G. Maxwell	(25,355)	Syed A. Hasan	(41,057)	John F. O'Rourke	(38,985)
William P. Christie	(29,371)	Kathleen M. Olster	(42,052)	Richard J. Paciulan	(28,248)
David A. Dillard	(30,831)	Daniel M. Cavanagh	(41,661)	Josephine E. Chang	(P-46,083)
Thomas J. Daly	(32,213)	Molly A. Holman	(40,022)	Albert J. Harnois, Jr.	(P-46,123)
Vincent G. Gioia	(19,959)	Lucinda G. Auciello	(42,270)	Steven E. Johnson	(P-45,916)
Edward R. Schwartz	(31,135)	Norman E. Carte	(30,455)	Frank L. Cire	(42,419)
John D. Carpenter	(34,133)	Joel A. Kauth	(41,886)	Harold E. Wurst	(22,183)
David A. Plumley	(37,208)	Patrick Y. Ikehara	(42,681)	Robert A. Green	(28,301)
Wesley W. Monroe	(39,778)	Mark Garscia	(31,953)		

doing business as the law firm CHRISTIE, PARKER & HALE, LLP, telephone 626/795-9900, as principal attorneys with power to appoint associate attorneys, to prosecute this application and any subsequent application based on the disclosure of this application, and to transact all business in the Patent and Trademark Office connected with this application and any subsequent application.

The authority under this Power of Attorney of each person named above shall automatically terminate and be revoked upon such person ceasing to be a member or associate of or of counsel to that law firm.

Please address all correspondence to CHRISTIE, PARKER & HALE, LLP, P.O. Box 7068, Pasadena, California 91109-7068.

Application No. Reissue of U.S. Patent No. 5,604,741

We declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First

Inventor : Henry Samueli

Inventor's Signature : \_\_\_\_\_

Residence Address : \_\_\_\_\_

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Citizenship : USA

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Inventor : Fang Lu

Inventor's Signature : *Fang Lu*

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Citizenship : Taiwan R.O.C.

JWE/mg

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Application No. Reissue of U.S. Patent No. 5,604,741

We declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First

Inventor

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Inventor's Signature

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Full Name of Second

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Citizenship

: USA

Full Name of Third

Inventor

: Fang Lu

Inventor's Signature

: \_\_\_\_\_

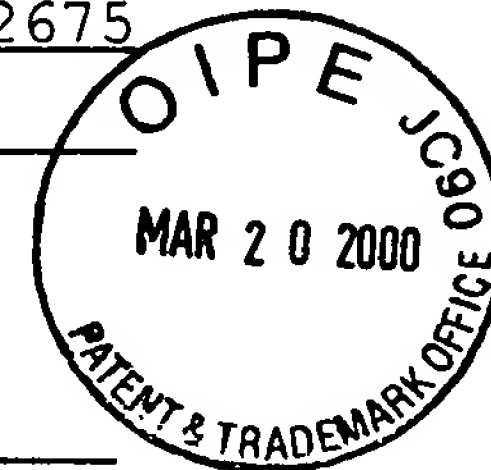
Residence Address

: 25 Arbusto

Irvine, California 92606

Citizenship

: Taiwan R.O.C.



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PATENT

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March 15, 2000.  
date

  
Signature



Applicant : Broadcom Corporation  
For : Reissue of U.S. Patent No. 5,604,741  
Issued : February 18, 1997  
Title : ETHERNET SYSTEM

Application No. : 09/252,551  
Filed : February 18, 1999

Docket No. : 34176/JWE/B600

**ASSIGNEE'S ASSENT, STATEMENT OF OWNERSHIP  
UNDER 37 CFR § 3.73(b) AND OFFER TO SURRENDER**

BOX REISSUE  
Assistant Commissioner for Patents  
Washington, D.C. 20231

P.O. Box 7068  
Pasadena, Ca. 91109-7068  
March 10, 2000

Commissioner:

Broadcom Corporation, a California corporation having a place of business at 16215 Alton Parkway, Irvine, California 92618, represents that it is the assignee of the entire interest in U.S. Patent No. 5,604,741, issued February 18, 1997, and entitled ETHERNET SYSTEM by virtue of an assignment recorded at reel 7369, frame 0419. Assignee hereby assents to the Application for Reissue of this patent for the same invention on the accompanying amended specification and claims.

Assignee hereby offers to surrender the original Letters Patent No. 5,604,741.

With this request is filed an order for title report, as required in such applications.

I declare that I am an officer of Broadcom Corporation, the assignee of the entire interest in U.S. Patent No. 5,604,741, and as



Application No. Reissue of U.S. Patent No. 5,604,741

such am empowered to act on behalf of assignee Broadcom Corporation. Such empowerment extends to the execution of this Assignee's Assent, Statement of Ownership and Offer to Surrender.

I declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements and the like, so made, are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and further that such willful false statements may jeopardize the validity of the application and any patent issuing thereon.

BROADCOM CORPORATION

Date

3/14/00

By

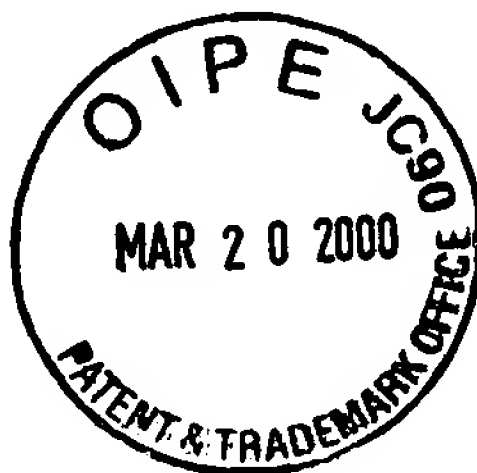
Henry Samueli

Henry Samueli  
(Name)

Co-Chairman of the Board,  
Chief Technical Officer  
(Title)

JWE/mg

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Applicant : Broadcom Corporation  
 For : Reissue of U.S. Patent No. 5,604,741  
 Issued : February 18, 1997  
 Title : ETHERNET SYSTEM  
 Application No. : 09/252,551  
 Filed : February 18, 1999

Docket No. : 34176/JWE/B600

# **SUPPLEMENTAL REISSUE DECLARATION**

BOX REISSUE  
 Assistant Commissioner for Patents  
 Washington, D.C. 20231

P.O. Box 7068  
 Pasadena, Ca. 91109-7068  
 May 14, 2001

Commissioner:

We, Henry Samueli, Mark Berman and Fang Lu, the below named inventors, hereby declare and state as follows:

1. This Supplemental Reissue Declaration supplements the Reissue Declaration and Power of Attorney dated March 10, 2000 executed by us with respect to claims 1 - 103 and 104 - 144.
2. Claims 133 - 135, 141 - 144, and 147 - 151 and 153 attached hereto which were submitted in amendments subsequent to the execution of, and correct the same error as indicated in, the above-referenced Reissue Declaration and Power of Attorney.
3. A statement of error is not needed since an error to support a reissue has been previously and properly stated in a reissue declaration in the application and that error is still being corrected in the reissue application.
4. Every error in the patent which was corrected in the present reissue application, and is not covered by the prior declaration submitted in this application, arose without any deceptive intent.
5. We declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are

**Reissue Application No. 09/252,551 of U.S. Patent No. 5,604,741**

believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First

Inventor

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Full Name of Second

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Full Name of Third

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: Fang Lu

Inventor=s Signature

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Residence Address

: Rowland Heights, CA.

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: Taiwan R.O.C.

133. A bidirectional data communication system comprising:  
communication signals having individual ones of a plurality of  
analog levels to represent information;  
a plurality of signal lines disposed in pairs and defining a  
multi-pair communication environment, each signal line transmitting or  
receiving said communication signals;  
a transmitter block, including a plurality of transmitters, each  
coupled to particular ones of the signal line pairs;  
a receiver block, including a plurality of receivers, each  
coupled to particular ones of the signal line pairs, each receiver  
including;  
an analog to digital converter configured to convert a  
plurality of analog levels into a corresponding plurality of digital levels  
defining a digital signal; and  
a fully digital adaptive equalizer coupled to the analog to  
digital converter and operating on the digital signal to define information  
represented by the plurality of digital levels;  
the receiver block further comprising timing recovery  
circuitry coupled to receive the digital signal from the analog to digital  
converter and extract timing information therefrom, the analog to digital  
converter operatively responsive to said timing information and performing  
digital conversions at a rate defined thereby;  
wherein the communication signals are provided in packets, each  
packet comprising a preamble portion and a data containing portion, the  
preamble portion including timing signals; and  
wherein the timing recovery circuitry comprises a first timing  
loop having a high gain stage and a second timing loop having a low gain  
stage, the first timing loop locking the analog to digital converter in  
phase with the preamble portion the second timing loop locking the analog to  
digital converter in phase with the data containing portion.

134. A bidirectional data communication system according to claim 133,  
wherein the first timing loop includes a high gain error generator, a loop  
filter, and an oscillator circuit, the high gain error generator responsive  
to characteristic values of the timing signals, and wherein the second  
timing loop includes a low gain error generator, a loop filter, and an

oscillator circuit, the high gain error generator responsive to characteristic values of the data signals.

135. A bidirectional data communication system comprising:
- communication signals having individual ones of a plurality of analog levels to represent information;
  - a plurality of signal lines disposed in pairs and defining a multi-pair communication environment, each signal line transmitting or receiving said communication signals;
  - a transmitter block, including a plurality of transmitters, each coupled to particular ones of the signal line pairs;
  - a receiver block, including a plurality of receivers, each coupled to particular ones of the signal line pairs, each receiver including:
    - an analog to digital converter configured to convert a plurality of analog levels into a corresponding plurality of digital levels defining a digital signal; and
    - a fully digital adaptive equalizer coupled to the analog to digital converter and operating on the digital signal to define information represented by the plurality of digital levels;
    - the receiver block further comprising timing recovery circuitry coupled to receive the digital signal from the analog to digital converter and extract timing information therefrom, the analog to digital converter operatively responsive to said timing information and performing digital conversions at a rate defined thereby;
    - the digital adaptive equalizer further comprising:
      - a feed forward equalizer having an input receiving the digital signal from the analog to digital converter and an output;
      - a slicer coupled to receive the digital signal from the feed forward equalizer and outputting a signal representing a symbol, the signal characterized by the digital levels;
      - an adder disposed between the feed forward equalizer and the slicer; and
      - a decision feedback equalizer having an input receiving the signal output by the slicer and an output coupled to the

adder, the adder summing the output of the decision feedback equalizer with the output of the feed forward equalizer.

141. A bidirectional data communication system comprising:  
communication signals having individual ones of a plurality of  
analog levels to represent information;  
a plurality of signal lines disposed in pairs and defining a  
multi-pair communication environment, each signal line transmitting or  
receiving said communication signals;  
a transmitter block, including a plurality of transmitters, each  
coupled to particular ones of the signal line pairs;  
a receiver block, including a plurality of receivers, each  
coupled to particular ones of the signal line pairs, each receiver  
including;  
an analog to digital converter configured to convert a  
plurality of analog levels into a corresponding plurality of digital levels  
defining a digital signal;  
an automatic gain control circuit coupled in feedback  
fashion to the analog to digital converter and operatively responsive to  
output signals therefrom to control the gain of received communication  
signals; and  
a fully digital adaptive equalizer coupled to the analog to  
digital converter and operating on the digital signal to define information  
represented by the plurality of digital levels;  
the digital adaptive equalizer further comprising:  
a feed forward equalizer having an input receiving  
the digital signal from the analog to digital converter and an output;  
a slicer coupled to receive the digital signal from  
the feed forward equalizer and outputting a signal representing a symbol,  
the signal characterized by the digital levels;  
an adder disposed between the feed forward equalizer  
and the slicer; and  
a decision feedback equalizer having an input  
receiving the signal output by the slicer and an output coupled to the  
adder, the adder summing the output of the decision feedback equalizer  
with the output of the feed forward equalizer.

142. A bidirectional data communication system according to claim 141, the receiver block further comprising timing recovery circuitry coupled to receive the digital signal from the analog to digital converter and extract timing information therefrom, the analog to digital converter operatively responsive to said timing information and performing digital conversions at a rate defined thereby.

143. A bidirectional data communication system according to claim 142, wherein the timing recovery circuitry comprises a first timing loop having a high gain stage and a second timing loop having a low gain stage, the first timing loop locking the analog to digital converter in phase with the preamble portion the second timing loop locking the analog to digital converter in phase with the data containing portion.

144. A bidirectional data communication system according to claim 143, wherein the first timing loop includes a high gain error generator, a loop filter, and an oscillator circuit, the high gain error generator responsive to characteristic values of the timing signals, and wherein the second timing loop includes a low gain error generator, a loop filter, and an oscillator circuit, the high gain error generator responsive to characteristic values of the data signals.

147. In a bidirectional communication system, a method of processing signals received through a multi-pair transmission medium, the signals having characteristic values occurring at a characteristic frequency, the method comprising:

providing an A/D converter, coupled to receive the signals from the transmission medium;

providing a sampling clock signal at a sampling clock frequency equal to the characteristic occurrence frequency of received signal characteristic values;

sampling the received signals in the A/D converter at the sampling clock frequency;



generating signal samples at the sampling clock frequency, each signal sample being output from the A/D at a time assumed to correspond to the occurrence of a signal characteristic value;

processing each signal sample in a timing recovery circuit coupled, in feedback fashion, between the output of the A/D and a sampling clock input thereto;

determining whether the occurrence of a signal characteristic value leads or lags the sampling clock signal in phase; and

adjusting the phase of the sampling clock signal such that each signal sample is output from the A/D at a time that actually corresponds to the occurrence of a signal characteristic value, a sampling clock phase thereby being locked to a corresponding phase of a signal characteristic value;

wherein the received signals are analog signals disposed in packets, each packet of the analog signals disposed in packets being divided into a first packet region comprising timing signals and a second packet region comprising data signals, the method further comprising:

sampling the received data signals in the A/D converter at the sampling clock frequency, wherein the data signals are sampled after the phase of the sampling clock signal has been locked to the phase of a signal characteristic value of the timing signals.

148. The method according to claim 147, wherein the data signals of each packet are characterized by a plurality of analog amplitude values, the values of the analog amplitudes defining information content, the analog amplitude values of the data signals being converted to digital representations thereof by the A/D converter after the phase of the sampling clock signal has been locked to the phase of a signal characteristic value of the timing signals.

149. The method according to claim 148, further comprising:

sampling the received data signals in the A/D converter at the sampling clock frequency;

generating data signal samples at the sampling clock frequency, each data signal sample being output from the A/D at a time assumed to



correspond to the occurrence of a signal characteristic value of the data signals;

processing each data signal sample in the timing recovery circuit;

determining whether the occurrence of a data signal characteristic value leads or lags the sampling clock signal in phase; and

adjusting the phase of the sampling clock signal such that the sampling clock phase is thereby locked to a corresponding phase of a data signal characteristic value.

150. The method according to claim 149, wherein the phase adjustment step adjusts the phase of the sampling clock signal in discrete amounts, and wherein the discrete amount of phase adjustment is greater when the phase adjustment step is performed in conjunction with the timing signals than when performed in conjunction with the data signals.

151. The method according to claim 147, wherein the first packet region comprises a particular number of timing signals and wherein the phase adjustment step is performed in operative response to a first subset of the particular number of timing signals.

153. In a bidirectional communication system, a method of processing analog signal packets received through a multi-pair transmission medium, each analog signal packet including a plurality of signals having characteristic values occurring at a characteristic frequency, the method comprising:

providing a sampling clock signal at a sampling clock frequency equal to the characteristic occurrence frequency of received signal characteristic values;

predicting an occurrence time corresponding to the characteristic occurrence frequency of received signal characteristic values;

sampling the received signals at the sampling clock frequency and at the predicted occurrence time to thereby generate signal samples at the sampling clock frequency, each signal sample assumed to correspond to the occurrence of a signal characteristic value;

processing the signal samples in a high gain error generator, the high gain error generator determining whether the occurrence of a signal characteristic value leads or lags the sampling clock signal in phase; and

adjusting the phase of the sampling clock signal such that each signal sample is generated at a time that actually corresponds to the occurrence of a signal characteristic value, the sampling clock having an occurrence time locked in phase with a corresponding occurrence of a signal characteristic value;

the signals of each analog signal packet being characterized by a plurality of analog amplitude values, the values of the analog amplitudes defining information content, the method further comprising:

dividing each analog signal packet into a first packet region comprising timing signals and a second packet region comprising data signals; and

converting the analog amplitude values of the data signals to digital representations thereof by an A/D converter after the occurrence time of the sampling clock signal has been locked to the occurrence time of a signal characteristic value of the timing signals.